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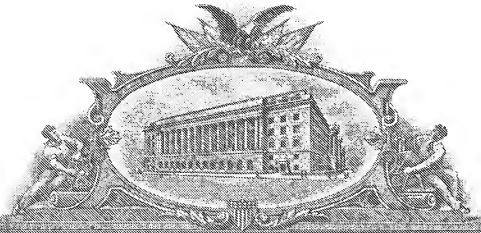

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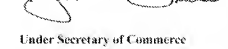

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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

Express Mail Label No. EV 509624126 US

INVENTOR(S)

Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
Frank D. Steven E.	Stroili Turner	Hollis, NH Westbrook, ME

Additional inventors are being named on the 1 *separately numbered sheets attached hereto*

TITLE OF THE INVENTION (500 characters max)

HIGH-SPEED 4-BIT ACCUMULATORS IMPLEMENTED IN INP DHBT TECHNOLOGY

Direct all correspondence to: **CORRESPONDENCE ADDRESS**

☑ Customer Number: 22500

OR

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ENCLOSED APPLICATION PARTS *(check all that apply)*

☑ Specification *Number of Pages* 9 ☐ CD(s), Number

☑ Drawing(s) *Number of Sheets* 3 ☐ Other (specify)

☐ Application Data Sheet. See 37 CFR 1.76

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT

☐ Applicant claims small entity status. See 37 CFR 1.27.

☐ A check or money order is enclosed to cover the filing fees.

☑ The Director is hereby authorized to charge filing fees or credit any overpayment to Deposit Account Number: 190130

☐ Payment by credit card. Form PTO-2038 is attached.

FILING FEE Amount ($): 160.00

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☐ No.

☑ Yes, the name of the U.S. Government agency and the Government contract number are: Army DAAD17-02-C-0115

Respectfully submitted,

SIGNATURE Daniel J. Long

TYPED or PRINTED NAME DANIEL J. LONG

Date 7/6/04

REGISTRATION NO. 29,404 *(if appropriate)*

Docket Number: 20040084 PRO

TELEPHONE 603-885-2643

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

PROVISIONAL APPLICATION COVER SHEET
Additional Page

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Docket Number	20040084 PRO

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Number 2 of 2

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EXPRESS MAIL CERTIFICATE EV 509624126 US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Stroili, et al.

Filed: Herein Atty. Dkt. No: 20040084 PRO

For: High Speed 4-Bit Accumulators Implemented In INP DHBT Technology

CERTIFICATE OF MAILING 37 CFR 1.10: I certify that this correspondence is being deposited on the below date with the U.S. Postal Service with sufficient postage as EXPRESS MAIL addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.

Date: 7-6-04 Gloria Abbasciano

Gloria Abbasciano

Dear Honorable Commissioner:

LETTER OF TRANSMITTAL

Submitted herewith is a Provisional Patent Application consisting of __1__ of cover sheet, __9__ pages of specification and claims,__3__sheets of drawings.

[X] Invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

DEPOSIT ACCOUNT **190130** AUTHORIZATION – The Office is hereby authorized to charge the required fee, and any deficiency or credit any overpayment in the fees to the above deposit account, owned by BAE SYSTEMS Information and Electronic Systems Integration Inc.

Respectfully submitted,

Daniel J. Long

Daniel J. Long, Reg. No. 29,404

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HIGH-SPEED 4-BIT ACCUMULATORS IMPLEMENTED IN INP DHBT TECHNOLOGY

Statement of Government Interest

The invention described herein was made under Contract No. DAAD17-02-C-0115 with the Government of the United States of America and may be manufactured and used by and for the Government of the United States of America for Governmental purposes without the payment of any royalties thereon or therefor.

Background of the Invention

1. Field of the Invention

The present invention relates to direct digital synthesizers used in an indium phosphide (InP) heterojunction bipolar transistor (HBT) process. More particularly this invention relates to high speed accumulators for use in such direct digital synthesizers.

2. Brief Description of Prior Developments

High-speed accumulator circuits are a critical component of direct digital synthesizers. Direct digital synthesizers are useful as a means for generating frequency-agile waveforms with complex modulation. To allow direct generation of these waveforms at radio frequencies up to X-band, the accumulator circuit must operate at clock rates $\geq$30GHz, thus they can benefit from the inherent high-speed of InP DHBT devices. The accumulator must also have a wide bit width in order to provide adequate frequency resolution, thus requiring transistor counts approaching 5000 devices. Such results based on the InP DHBT process are disclosed in G. He, J. Howard, M. Le, P. Partyka, B. Li, G. Kim, R. Hess, R. Bryie, R. Lee, S. Rustomji, J. Pepper, M. Kail, M.

Helix, R. Elder, D. Jansen, N. E. Harff, J. Prairie, and E. S. Daniel, "Self-aligned InP DHBT with f_t and f_{max} both over 300 GHz in a new manufacturable technology," *IEEE Electron Device Letters*, 2004, submitted for publication. This process has f_t and f_{max} both over 300 GHz, and uses a self-aligned 0.35 μm device structure that provides improved yield and manufacturability on large device count circuits.

We previously reported test results of a fabricated InP 4-bit accumulator operating at 41GHz with a power consumption of 4.1W as is disclosed in S. E. Turner, D. S. Jansen, and D. E. Kotecki, "4-bit adder-accumulator at 41 GHz clock frequency in InP DHBT technology," *IEEE Microwave and Wireless Components Letters*, 2004, submitted for publication, the contents of which are incorporated herein by reference. This design used a multi-level circuit topology requiring a 5.5V supply voltage for some critical sub-circuits, which leads to the relatively high power dissipation.

Summary of Invention

As an alternative to such prior developments , we have developed a circuit that allows the overall power supply voltage to be reduced by a diode drop, while maintaining high clock frequency operation. Simulations of a 4-bit accumulator with this new circuit show operation at 40GHz clock frequency with a power consumption of 3.4W. In both instances, the circuits are designed for maximum speed and operate near peak f_t. This application discloses the architecture of the accumulator, the design of the previously reported circuit, and the modifications contained in the new benchmarks.

Brief Description of the Drawings

The present invention is further described in the accompanying drawings wherein:

Figure 1 is a schematic drawing showing cascadable accumulator architecture;

Figure 2 is a schematic drawing showing 2-bit adder;

Figure 3 is a schematic drawing showing single-level parallel-gated carry circuit;

Figure 4 is a schematic drawing showing three-level series-gated sum circuit; and

Figure 5 is a schematic drawing showing extracted simulation of the DAC output of the accumulator test circuit with an accumulation increment of 7, operating at 40GHz wherein digital values corresponding to the analog output are superimposed on the figure.

Detailed Description of the Preferred Embodiment

Accumulator Architecture

The accumulator architecture as is disclosed in C. G. Eckroot and S. I. Long, "A GaAs 4-bit adder-accumulator circuit for direct digital synthesis," *IEEE Journal of Solid State Circuits*, vol. 23, no. 2, pp. 573-580, Apr. 1988, uses 2-bit adder blocks which are cascadable to any 2N-bit width as shown in Figure 1. The cascaded architecture allows for wide bit-width accumulators without much of a speed penalty, since the frequency of operation is determined by the feedback of the sum and the setup time of the carry input. As the bit-width increases, the total number of accumulators increases linearly, while the total number of registers increases in a quadratic fashion:

$$\#accumulators = \frac{bits}{2}$$

$$\#registers = \frac{bits^2}{8} - \frac{bits}{4}$$

As a result, the power consumption of the registers becomes a dominant factor for accumulators with large bit-widths.

The individual 2-bit adder blocks contain internal pipelining and an architecture that merges the logic and latching functions T. Mathew, S. Jaganathan, D. Scott, S. Krishnan, Y. Wei, M. Urtega, M. Rodwell, and S. Long, "2-bit adder carry and sum logic circuits clocking at 19 GHz clock frequency in transferred substrate HBT technology," in *Proceedings of IEEE International Conference on Indium Phosphide and Related Materials*, Nara, Japan, May 2001, pp. 505-508, and T. Mathew, S. Jaganathan, D. Scott, S. Krishnan, Y. Wei, M. Urtega, M. J. W. Rodwell, and S. Long, "2-bit adder: carry and sum logic circuits at 19 GHz clock frequency in InAlAs/InGaAs HBT technology," *Electronics Letters*, vol. 37, no. 19, pp. 1156-1157, Sept. 2001. The 2-bit adder block is shown in Figure 2. The carry and sum blocks contain both logic functionality and latches, thus the clock inputs control these internal latches. The left and right sides of the adder are driven by opposite clock phases, resulting in the computation and latching of a full 2-bit add operation in a single clock cycle.

Accumulator with Modified Carry Circuit

In prior work T. Mathew, S. Jaganathan, D. Scott, S. Krishnan, Y. Wei, M. Urtega, M. Rodwell, and S. Long, "2-bit adder carry and sum logic circuits clocking at 19 GHz clock frequency in transferred substrate HBT technology," in *Proceedings of IEEE International Conference on Indium Phosphide and Related Materials*, Nara, Japan, May 2001, pp. 505-508, and T. Mathew, S. Jaganathan, D. Scott, S. Krishnan, Y. Wei, M. Urtega, M. J. W. Rodwell, and S. Long, "2-bit adder: carry and sum logic circuits at 19 GHz clock frequency in InAlAs/InGaAs HBT technology," *Electronics Letters*, vol. 37, no. 19, pp. 1156-1157, Sept. 2001, the carry and sum circuits both require four series-gated levels, while registers only require two series-gated levels. Unless multiple power

supplies are utilized, the extra levels translate into unnecessary power consumption in the registers. An initial attempt at solving this problem S. E. Turner, R. B. Elder, D. S. Jansen, and D. E. Kotecki, "4-bit adder-accumulator at 41 GHz clock frequency in InP DHBT technology," *IEEE Microwave and Wireless Components Letters*, 2004, submitted for publication. gave rise to the modified carry circuit shown in Figure 3. Instead of using four-level series-gated logic, this design used single-level parallel-gated logic. Theoretically, this would enable operation at a supply voltage as low as 3.6V. However, additional diodes are added to the carry circuit to preserve logic level compatibility with other circuits in a test chip implementation with a single power supply.

Although the use of the four-level series gated sum circuit prevents the design from taking advantage of power reduction, the 4-bit accumulator constructed with the modified carry circuit showed promising results. Using InP DHBT technology with f_t and f_{max} both over 300GHz, G. He, J. Howard, M. Le, P. Partyka, B. Li, G. Kim, R. Hess, R. Bryie, R. Lee, S. Rustomji, J. Pepper, M. Kail, M. Helix, R. Elder, D. Jansen, N. E. Harff, J. Prairie, and E. S. Daniel, "Self-aligned InP DHBT with f_t and f_{max} both over 300 GHz in a new manufacturable technology," *IEEE Electron Device Letters*, 2004, submitted for publication. We were able to realize a 4-bit accumulator test circuit with 624 transistors at a maximum clock frequency of 41GHz and an overall power consumption of 4.1W. Note that this power consumption figure is for the whole test circuit, including supporting circuitry such as the DAC used for output. The accumulator core by itself (two 2-bit adders, one 2-bit register, and clock tree) requires 2.86W.

Accumulator with Modified Carry and Sum Circuits

In order to reduce the power consumption of the design, the three-level series-gated sum circuit of Figure 4 has been developed. Since the previous sum circuit was the only portion of the circuit constraining the design to a power supply supporting four series-gated levels, this new design allows for overall power reduction. This is achieved by the removal of one diode drop from the power supply and other circuitry in the test chip such as the carry circuit of Figure 3. The registers in the pipeline benefit from this change in terms of power consumption, particularly in designs with large bit-widths.

A 4-bit accumulator test circuit with a single-level parallel-gated carry circuit and a three-level series-gated sum circuit has been designed and taped-out for fabrication. Simulations of a 4-bit accumulator test circuit, including extracted parasitics, showed a maximum clock frequency of 40GHz. The test circuit includes an on-chip DAC that allows for observation of a single output using a high-speed sampling oscilloscope. Figure 5 shows a simulation of the DAC output of the test circuit operating at 40GHz with an accumulation increment of 7. The digital values corresponding to the analog output are superimposed on the figure. Power consumption was simulated at 3.7W for the whole test circuit and 2.38W for the accumulator core (two 2-bit adders, one 2-bit register, and clock tree).

Conclusion

In our previous work, we were able to demonstrate the inherent speed and yield of the InP DHBT process by demonstrating an accumulator test circuit operating at a 41GHz clock frequency with over 600 transistors. By modifying the sum circuit and reducing the power supply from our previous design, we were able to simulate a reduction in the

core power consumption of over 16% while maintaining high frequency operation at 40GHz. While this work was designed near peak f_t for maximum speed performance, further reductions in power can be made by reducing the supply voltage to 3.6V and decreasing the current density at the expense of a lower clock frequency of 30GHz.

While the present invention has been described in connection with the preferred embodiments of the various figures, it is to be understood that other similar embodiments may be used or modifications and additions may be made to the described embodiment for performing the same function of the present invention without deviating therefrom. Therefore, the present invention should not be limited to any single embodiment, but rather construed in breadth and scope in accordance with the recitation of the appended claims.

Claims

What is claimed is:

1. A method for operating a high-speed 4-bit accumulator in an indium phosphide (InP) heterojunction bipolar transistor (HBT) process, wherein the improvement comprises using 624 transistors while maintaining a 40 GHz operating frequency, whereby a 16% power reduction is obtained.

Abstract

High-speed accumulators are frequently used as a benchmark of the ability to yield large scale circuits in high speed InP double hetereojunction bipolar (DHBT) processes. In previous work, we reported test results of an InP DHBT 4-bit accumulator with 624 transistors operating at 41GHz clock frequency with a power consumption of 4.1W. In this work, we report on modifications that allow the circuit to operate at a lower supply voltage. Simulation results for one modification indicate that a 16% power reduction can be obtained, while maintaining a 40GHz operating frequency.

Drawings

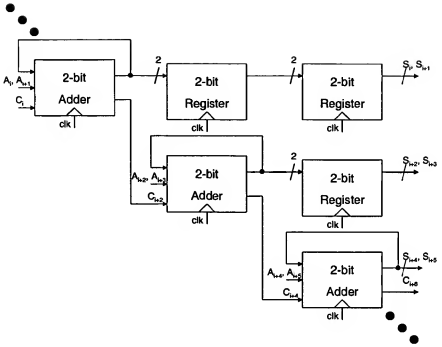

Figure 1

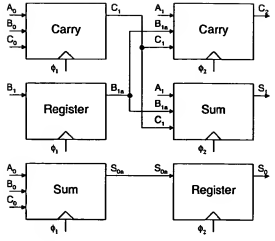

Figure 2

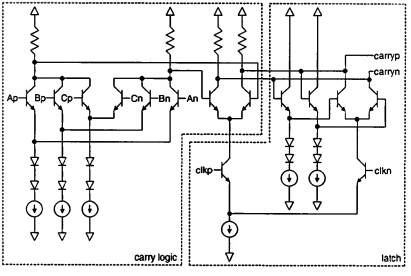

Figure 3

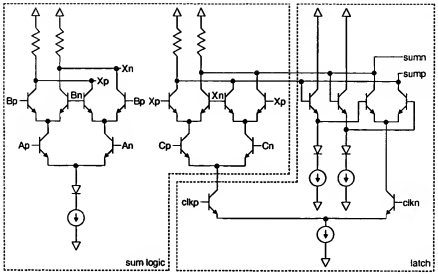

Figure 4

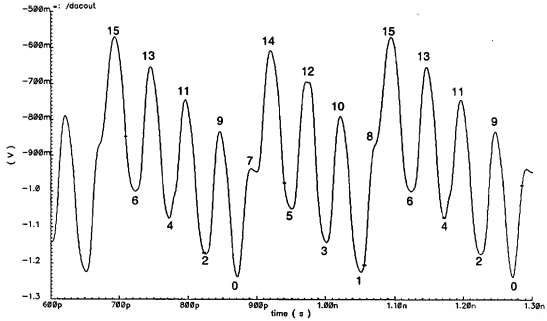

Figure 5